REMARKS

Claims 1-26 have been presented for examination. Applicant would like to thank the Examiner for identifying the allowable subject matter.

Objections to the Specification

The specification is objected to because of certain informalities. The specification has been amended to remove the informalities.

Claim Rejections under 35 USC §102(b)

Claims 1, 17 and 20-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by US patent No. 5,892,768 ("Jeng"). Applicants respectfully traverse these rejections.

To anticipate a claim, the reference must teach all limitations of the claim. *See* MPEP §2131. As to claim 1, Jeng does not teach each and every limitation of claim 1. The Examiner has cited an Ethernet port 40 containing a dual MAC 44 as anticipating a first IC and a second IC as recited in claim 1. Applicants respectfully disagree. The MAC 44 is a single IC containing dual MACs 46, 48 (*see* figure 2). In fact, Jeng even provides an example of an industrial part to implement the dual MAC and dual buffer memories. According to Jeng, "[t]he dual MAC and dual buffer memories can be implemented using the model MX9742 MAC bridge controller manufactured by Macronix." (Col. 3, lines 65-67). Thus, Jeng does not disclose a first IC and a second IC as recited in claim 1.

Further, according to Jeng, The dual MACs in combination with dual buffer memories receive, store, and process packets/frames (*see* col. 4, lines 1-12). In contrast, claim 1 recites a first integrated circuit (IC) including **one or more receivers** and a second IC including **one or more transmitters**. In the cited sections, Jeng does not teach this limitation. Accordingly, Jeng does not teach each and every limitation of claim 1 as required under 35 USC §102(b) to anticipate a claim. Thus, claim 1 is patentably distinguishable from Jeng.

Claims 17 and 20-22 have been rejected in the manner of claim 1. Accordingly, claims 17 and 20-22 are patentably distinguishable from Jeng for at least the same reasons as claim 1.

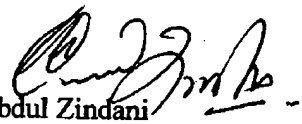
Claim Rejections under 35 USC §102(e)

Claim 11 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by US patent No. 6,490,727 ("Nazarathy et al"). Applicants respectfully traverse these rejections.

To anticipate a claim, the reference must teach all limitations of the claim. *See* MPEP §2131. As to claim 11, Nazarathy et al. do not each and every limitation of claim 11. The Examiner has cited figure 20 as describing each limitation of claim 11 including a central processing unit, which according to the Examiner, is "included in the Interactive Agent in fiber node 194." (Emphases added). However, a careful reading of the cited section reveals that Nazarathy et al. do not include Interactive Agent in the fiber node 194 shown in figure 20 and have actually replaced the Interactive Agent in the fiber node 194 with a LAN/WAN Gateway 456-1, and 456-2. According to Nazarathy et al., "...the AGs 190 described above in the deep fiber nodes are **replaced by a Modem Bank or LAN/WAN Gateway 456-1, 456-2** that on one side couples to the input/output of a full-duplex digital signal channel ..." (col. 36, lines 8-11, emphasis added). Thus, Nazarathy et al. do not teach each an every limitations as recited in claim 11 as required under 35 USC §102(b) to anticipate a claim. Accordingly, claim 11 is patentably distinguishable from Nazarathy et al.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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